REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-14 remain in the application. Claims 1, 10, and 14 have been amended.

Independent claims 10 and 14 have been amended to recite a semiconductor device(s) for performing the method of claim 1.

Applicants appreciatively acknowledge the Examiner's statement that claims 8 and 9 are allowed.

In the paragraph under "Drawings" on page 2 of the above-identified Office Action, the Examiner objected to the drawings because they fail to show DDR interface as described in the instant specification.

The DDR interface is described in detail in the instant specification (for example, see page 4, lines 11-25 and page 13, line 18 to page 14, line 2) and describes an interface with a "double data rate." Such an interface is present for example in the semiconductor device 1 and in Figs. 1 and 3 at the junction of the control and address bus CA with the data bus DQ, that is, at the terminals 21, 22. The DDR interface

can thus be reproduced for example with the terminals 21, 22. There is nothing more to be shown in the drawings since the DDR interface is fully described in the instant specification.

In view of the foregoing, nothing further has to be shown in the drawings and the Examiner is requested to withdraw the objection to the drawings.

In the paragraph under "Specification" on page 3 of the above-identified Office Action, the Examiner objected to the specification because element 42 shown in Fig. 3 is not found in the instant specification.

Applicants respectfully point out that reference number 42 is specifically mentioned in the specification as an "auxiliary path" on page 15, lines 15-18 of the instant specification.

Therefore, the Examiner is requested to withdraw the objection.

In Claim Rejections - 35 USC 112", the Examiner has rejected claim 7 as being indefinite.

More specifically, the Examiner states that ' a reaction to an operation condition" is not clear.

Applicants disagree with the Examiner and submit that the recitation in claim 7 is definite and supported by the instant specification. It is apparent from the original disclosure including line 17, page 8 to line 22, page 11 of the instant specification that the reaction is an electronic reaction to an operating condition of a semiconductor device.

In view of the foregoing, applicants do not believe that any amendment to claim 7 is required.

In the paragraph under "Claim Objections" on page 3 of the above-identified Office Action, claims 1 and 7 have been objected to because of certain informalities.

The Examiner's suggested correction has been made in claim 1. The feature set forth in claim 7 is described, for example, in lines 12-15 on page 8 of the instant specification.

Applicants submit that the feature of claim 7 is clearly and fully described in the instant specification as noted above and the Examiner's objection has been addressed and overcome. Therefore, the Examiner is requested to remove the objection to claim 7.

In the second paragraph under "Claim Rejections - 35 USC § 103" on page 4 of the above-identified Office Action, claims 1-2 and 5-6 have been rejected as being unpatentable over Wyers et al. (US 2004/0201416 A1) (hereinafter "Wyers") under 35 U.S.C. § 103(a).

In the fourth complete paragraph under "Claim Rejections 35 USC § 103" on page 6 of the above-identified Office Action, claims 3-4 have been rejected as being unpatentable over Admitted Prior Art ("APA") and Wyers and further in view of Yada (US 4,559,521) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Applicants respectfully note that the Wyers et al. U.S. Patent Application Publication No. 2004/0201416 has an effective date as a reference of **April 11, 2003.** See 35 U.S.C. § 102(e). As set forth in the Declaration of record, the instant application claims international priority of the **German Application No. 102 45 536.8**, filed **September 30, 2002**, under 35 U.S.C. § 119. Pursuant to 35 U.S.C. §§ 119, applicants are entitled to the priority date of the aforesaid German application. See MPEP §§ 201.13 and 1895. Thus, the instant

application predates Wyers et al. by more than six months. Because Wyers et al. was filed after the priority date of the instant application, applicants respectfully believe that Wyers et al. is unavailable as prior art.

Applicants acknowledge that perfection of priority can only be obtained by filing a certified English translation of the German priority application. See 35 U.S.C. § 119. Applicants previously have filed a Claim for Priority (filed December 3, 2003) and a certified copy of German Application No. **102 45 536.8** and now encloses a certified English translation of same. Accordingly, applicants respectfully believe that priority has been perfected and Wyers et al. is unavailable as prior art. Therefore, applicants respectfully submit that the Section 103 rejections on pages 4 and 6 of the Office Action are now moot and requests that the Examiner withdraw the rejections.

In the second complete paragraph under "Claim Rejections 35 USC § 103" on page 7 of the above-identified Office Action, claims 10-14 have been rejected as being unpatentable over Admitted Prior Art in view of Yada under 35 U.S.C. § 103(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the

instant application. Support for the changes is found in the original claims of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 10 calls for, *inter alia*, a semiconductor device:

the device for performing the calibration according to claim 1;

control and address connections for connecting to a control and **address bus**;

data connections for connecting to a data bus;

a calibration connection for connecting to a calibration reference;

an instruction evaluation unit connected to the control and address connections;

a calibration path;

a calibration unit connected to the calibration connection through the calibration path;

a calibration signal path; and

a switching unit integrated in the calibration path for opening and closing the calibration path, the switching unit coupled to the instruction evaluation unit through the calibration signal path, the instruction evaluation unit controlling the switching unit on a basis of calibration instructions transmitted via the control and **address bus**. (emphasis added)

In the Examiner's arguments in rejecting the claims, prior art Fig. 1 is compared with the present invention shown in Fig. 3 of the instant application. As a result, the Examiner recognizes that the switching unit 4 with the calibration path 41, 42 is a distinguishing difference between the prior art and the invention according to the instant application. The Examiner then proceeds, on the basis of hindsight, to take a controlled switch in a signal path from Yada (see the dashed arrows in Fig.2 between the switch control 37 and the switches 21, 22, and between the switch control 32 and the switch 13) and attempt to modify the Admitted Prior Art shown in Fig. 1 of the instant application..

However, it is noted that Yada shows an A/D converter and does not show or suggest a method for calibrating interface devices using the method according to the present invention which pertains to data transmission in data bus systems.

Clearly, the references do not show "a device for performing the calibration according to claim 1; control and address connections for connecting to a control and address bus" and "data connections for connecting to a data bus" and "said instruction evaluation unit controlling said switching unit on a basis of calibration instructions transmitted via the control and address bus" as recited in claim 10 of the instant application. Independent claim 14 contains similar limitations.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 10 or 14. Claims 10 and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 10.

In view of the foregoing, reconsideration and allowance of claims 1-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

F. Donald Paris (24,054)

FDP/bb

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101